CLAIMS

[1] A multiple-supply-voltage semiconductor device comprising a plurality of blocks, any or all of which have an independent clock circuit, and operating with a plurality of power supply voltages, characterized in that:

a variable delay circuit which provides an amount of delay changing in accordance with a power supply voltage is provided for any or all of clock signals each of which is provided from a clock generator circuit to each of the plurality of blocks.

[2] The multi-supply-voltage semiconductor device according to claim 1, wherein the variable delay circuit increases the amount of delay as the power supply voltage decreases.

[3] A multi-supply-voltage semiconductor device comprising a plurality of blocks, any or all of which have an independent clock circuit, and operating with a plurality of power supply voltages, characterized in that:

a voltage level detector circuit which detects the voltage level of the power supply voltage and outputs the detected voltage level as a voltage level detect signal is provided; and

a variable delay circuit which changes an amount of delay in accordance with the voltage level detect signal is provided for any or all of clock signals each of which is provided from a clock generator circuit to each of the plurality of blocks.

[4] A multi-supply-voltage semiconductor device comprising a plurality of blocks, any or all of which have an independent clock circuit, and operating with a plurality of power supply voltages, characterized in that:

a phase synchronizing circuit for bringing the clock signals in the blocks into phase is provided for any or all of clock signals each of which is provided

from a clock generator circuit to each of the plurality of blocks.

[5] The multi-supply-voltage semiconductor device according to claim 4, wherein a variable delay circuit which provides an amount of delay changing in accordance with the power supply voltage to compensate for a change in delay of a level shifter is provided for any or all of the phase synchronizing circuits, the level shifter adjusting a signal level between blocks supplied with different power supply voltages.

[6] The multi-supply-voltage semiconductor device according to one of claims 1 to 5, further comprising:

a voltage change detector circuit which detects a change in the power supply voltage; and

blocking means for blocking a clock signal generated by the clock generator circuit from being supplied to each of the block circuits during a period in which the voltage change detector circuit determines that a voltage is changing.

[7] The multi-supply-voltage semiconductor device according to one of claims 1 to 5, further comprising:

a minimum voltage detector circuit which generates and outputs a power supply control signal which provides control to minimize the power supply voltage within a range in which a normal operation can be performed at a predetermined clock frequency; and

a power supply control circuit which controls the power supply voltage in accordance with the power supply control signal.

[8] A multi-supply-voltage semiconductor device comprising a plurality of blocks, any or all of which have an independent clock circuit, and operating with a plurality of power supply voltages, characterized in that:

a power supply control circuit which controls the power supply voltage in

accordance with an operation mode signal indicating the current operation mode is provided; and

a variable delay circuit which changes an amount of delay in accordance with the operation mode signal is provided for any or all of clock signals each of which is provided from a clock generator circuit to each of the plurality of blocks.

[9] The multi-supply-voltage semiconductor device according to claim 8, further comprising:

a mode change detector circuit which, when detecting a change of the operation mode indicated by the operation mode signal, forces and keeps a clock control signal to a predetermined value for a given period of time set by a timer contained in the mode change detector circuit; and

blocking means for blocking a clock signal generated by the clock signal generator circuit from being supplied to each of the block circuits while the clock control signal is kept at the predetermined value.